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ORIGINAL CONTRIBUTION

Design Level Shifted Multicarrier Techniques for Cascaded H-Bridge Sub-Multilevel Inverter

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***Abstract*— The key aim of this paper is to implement and analyze level-shifted multicarrier techniques in Cascaded H Bridge (CHB) - Sub multi-level inverter to produce multiple level output voltage. The multi-level inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. The asymmetrical DC voltage sources are used for CHB Sub-Multilevel inverter, and the 15-level output voltage is obtained. The asymmetrical DC voltage Sources 12V, 24V, and 48V are used to get the 15 Level output voltage. The multicarrier Pulse Width Modulation (PWM) is used to get the desired voltage at the output. The Level Shifted Phase Disposition (LSPD) and Level Shifted Phase Opposition Disposition (LSPOD) multicarrier PWM techniques are used to reduce the Total Harmonic Distortion (THD) in the output voltage. The circuit is developed and analyzed in MATLAB software. The THD, measured by using the FFT tool of MATLAB software From the simulated results, the level-shifted phase opposition disposition multicarrier PWM has better performance than level-shifted phase disposition multicarrier PWM technique because it contains fewer harmonics so to improve the system reliability and quality. The performance analysis and mitigation of harmonics can enhance the power quality of the supply voltage delivered to the customers. However, power quality occurs several problems such as voltage sag, swell, under-voltage, overvoltage, transients, etc.**

***Index Terms*— CHB Sub-MLI, Asymmetric, LSPD, LSPOD**

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I. INTRODUCTION

Power electronics inverters have become a core element of the modern high-tech world. They have been applied for various uses, i.e., flexible AC transmission systems and electrical automobiles [1, 2, 3, 4]. Most of the multi-level inverter applications are finding in the UPS (Unprintable power supply), electric vehicle, and grid-connected system. The multi-level inverters have a higher number of output voltage levels than any other formal inverter and with accurate (to the best approximation) sinusoidal waveform. They are highly efficient due to high switching frequency, reduced harmonics in output, small size, reduced DV/dt, and high electromagnetic compatibility [5, 6, 7].

The conventional multi-level inverters have been classified into three types. They are Flying Capacitor, Neutral Point Clamped, and Cascaded H-Bridge multi-level inverters. The CHB multi-level is mostly used to require a huge amount of power for industrial applications [8, 9, 10, 11]. For switching control in CHB-Multilevel Inverters, different techniques are used like Level-Shifted, Phase-Shifted, Level-Shifted Phase Disposition, Level-Shifted Phase Opposition Disposition and Alternate Phase Opposition Disposition [12, 13, 14]. Different PWM techniques are used to get the desired output voltage level of sinusoidal output.

To improve power system reliability and quality, new techniques are introduced. As the number of voltages level increases, the harmonics decrease. Multi-level Inverters are used to enhance the output voltage waveform near the sinusoidal waveform by reducing the harmonic. Due to their non-sinusoidal output, these converters have generated harmonics in output voltage. To improve output voltage waveform, multi-level inverters are implemented through numerous control techniques to enhance the waveforms. These control methods such as Space Vector Modulation (SVM), Sinusoidal Pulse Width Modulation (SPWM), and Selective Harmonics Elimination Pulse Width Modulation (SHE PWM) employed to assess the output voltage of converters [15, 16, 17]. As equipment, undergone impressive developments in the industry and utility networks, the different stages of the converter have progressed. It also works with high performance and low maintenance costs [13, 18, 19]. The performance analysis and mitigation of harmonics can enhance the power quality of the supply voltage delivered to the customers. However, power quality occurs several problems such as voltage sag, swell, under-voltage, over-

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voltage, transients, etc. [13, 20, 21]. The critical source of harmonics in power converters is the usage of solid-state devices, i.e., non-linear devices. In this regard, the primary concern is to determine the most effective method to reduce harmonics produced in multi-level inverters [22]. Thus, this research gap highlights the best applicable technique by using MATLAB software in CHB Sub-Multilevel inverter by implementing the Multi-carrier PWM techniques, Level-Shifted Phase Disposition and Level Shifted Opposition Disposition to get the 15 levels at the output by using asymmetrical DC sources.

II. METHODOLOGY

. *Operation Principle of Cascaded H-Bridge Sub-Multilevel Inverter*

Sub-MLI produces a more significant output voltage level with less number of DC sources and switching devices. It consists of a level generator and polarity changer. The levels generated with subcells of cascaded bridge and polarity is changed with H bridge inverter shown in Fig. 1. In this Fig. 7 switches (IGBT), three diodes and three asymmetrical voltage sources (12V, 24V and 48V) are used to get the 15 level output.

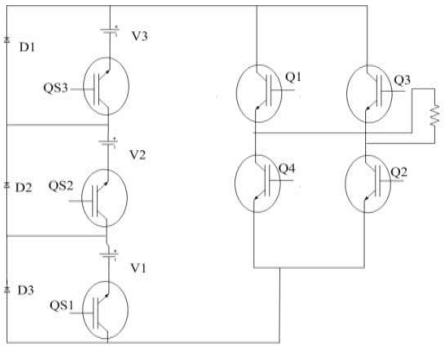

Fig. 1. Proposed topology of CHB sub-multilevel inverter

1) Positive cycle operation of CHB Sub-Multilevel Inverter: In the positive cycle of the CHB Sub-MLI the switches QS1, QS2, QS3, Q1 and Q2 are on while Q3 and Q4 are off and 0-level can be generated all the switches of CHB Sub-MLI, as described in Table. I.

TABLE I
POSITIVE CYCLE OPERATIONS

Level	QS1	QS2	QS3	Q1	Q4	Q3	Q2	Output
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1	VDC
2	0	1	0	1	0	0	1	2VDC
3	0	1	1	1	0	0	1	3VDC
4	1	0	0	1	0	0	1	4VDC
5	1	0	1	1	0	0	1	5VDC
6	1	1	0	1	0	0	1	6VDC
7	1	1	1	1	0	0	1	7VDC

2) Negative Cycle Operation CHB Sub-Multilevel Inverter: In the negative cycle of the CHB Sub-MLI, the switches QS1, QS2, QS3, Q4 and Q3 are on while Q1 and Q2 are off, as described in Table II.

TABLE II
NEGATIVE CYCLE OPERATION

Level	QS1	QS2	QS3	Q1	Q4	Q3	Q2	Output
8	0	0	0	0	0	0	0	-VDC
9	0	0	1	1	0	0	1	-2VDC
10	0	1	0	1	0	0	1	-3VDC
11	0	1	1	1	0	0	1	-4VDC
12	1	0	0	1	0	0	1	-5VDC
13	1	0	1	1	0	0	1	-6VDC
14	1	1	0	1	0	0	1	-7VDC

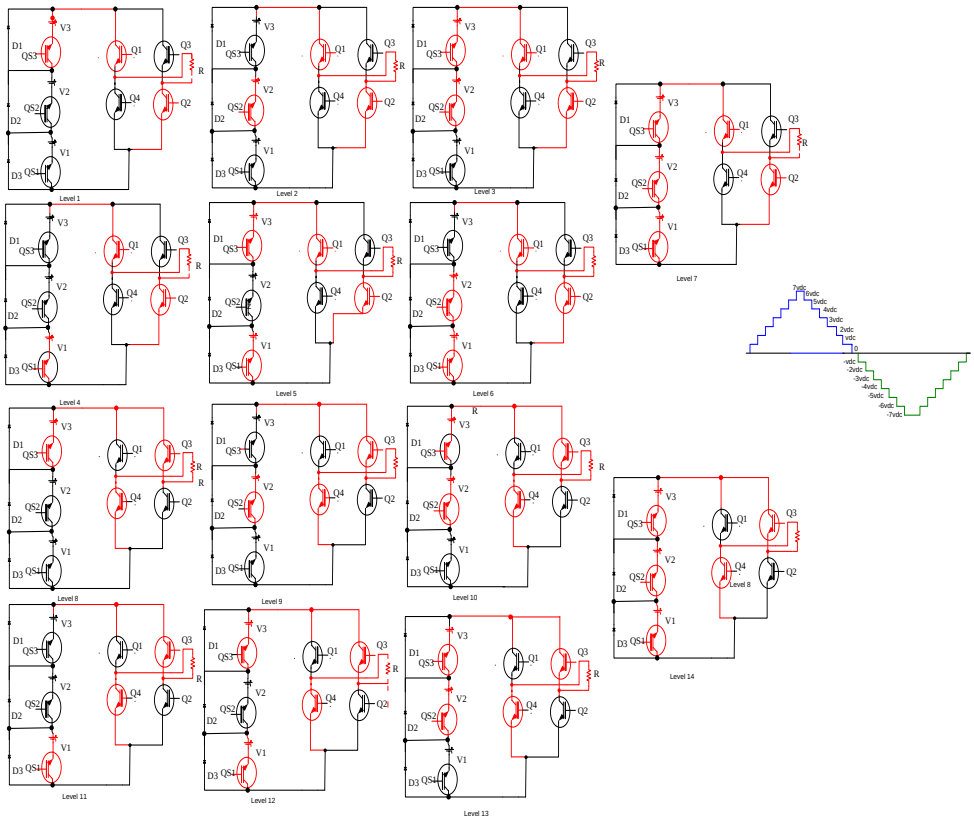

Fig. 2. Negative and positive cycle operation and 15 Level output voltage waveform of CHB Sub-MLI

Fig. 2 shows the switching of proposed topology (Red colour indicates the switches are ON whereas the black colour shows the switches are OFF), above figure, described as in positive cycle at the level 1 VDC (output voltage), level 2 2VDC(Output Voltage), level 3 3VDC (output Voltage), level 4 4VDC (output Voltage), level 5 5VDC (output Voltage), level 6 6VDC (output Voltage, level 7 7VDC (output Voltage) and in negative cycle operation at level 8 - VDC (Output Voltage), level 9 - 2VDC (output Voltage), level 10 - 3VDC (output Voltage), level 11 - 4VDC (output Voltage), level 12 - 5VDC (output Voltage), level 13 - 6VDC (output Voltage) and at level 14 - 7VDC (output Voltage) are obtained to get 15 levels at the output.

B. PWM Multicarrier Level Shifted Modulation Techniques

PWM multicarrier techniques are implemented to get the desired voltage at the output side of the inverter. PWM techniques were classified in Level Shifted, Phase-Shifted, and Variable Frequency Implement in MLI [22]. Whereas in this work 14 carrier waveforms of PWM are used to get the 15 levels at the output of voltage, by implementing the Level Shifted Phase Disposition and Level Shifted Phase Opposition Disposition multicarrier PWM.

1) Level shifted phase disposition multicarrier PWM: In level-shifted phase disposition there 14 carrier waveform's that are in phase with the reference signal, having the same magnitude and frequency.

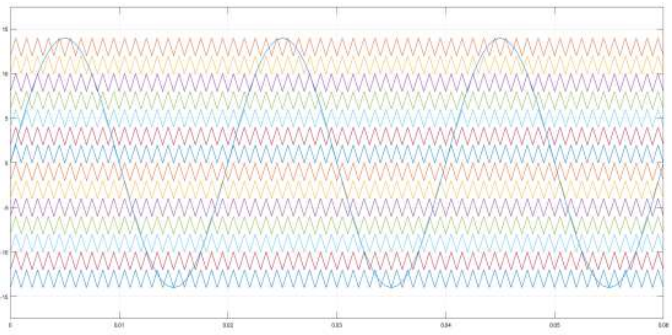

Fig. 3. The output of level-Shifted PD MCPWM

2) Control signals of LSPD MCPWM: Multicarrier waveforms of level obtain 14 Control signals, Level shifted multicarrier phase disposition PWM to get the 15 level output.

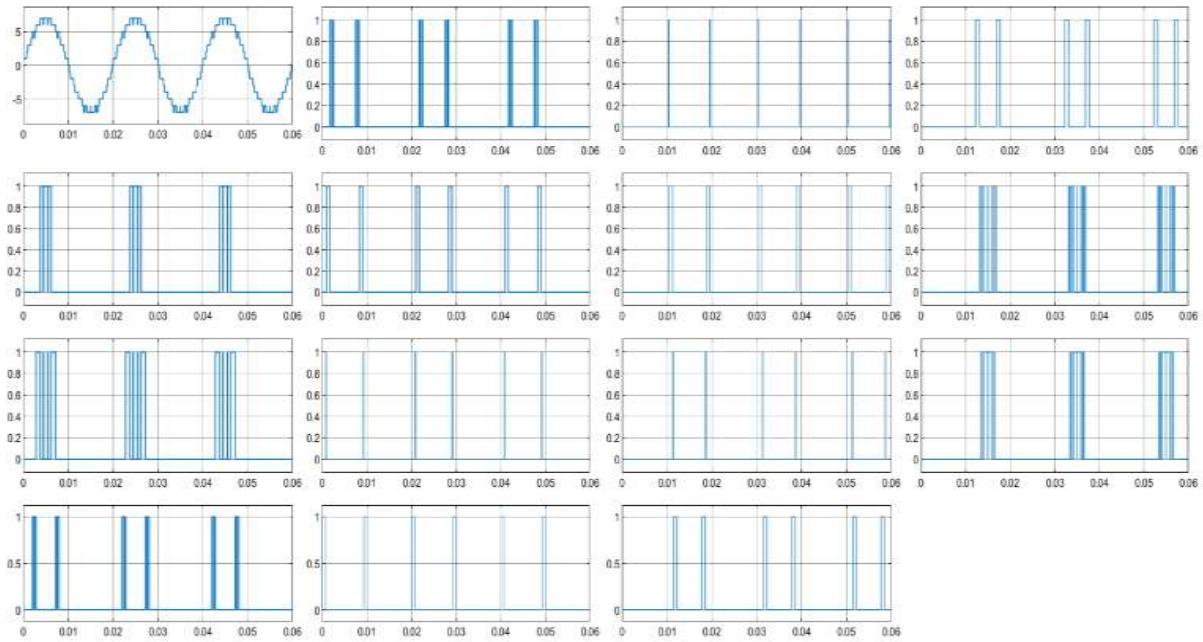

Fig. 4. Control Signals of LS PD MCPWM

3) Level shifted Phase Opposition Disposition Technique: There are 14 carrier waveforms of the Level-Shifted Phase Opposition Disposition. They are phase-shifted by 180 degrees between waveforms above and below zero, but the reference signal's value is the in-phase. This technique is used to get the desired voltage at the output.

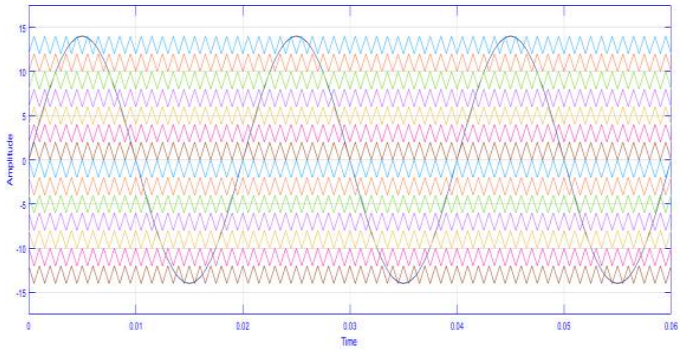

Fig. 5. Output Waveforms of POD MC PWM

4) Control signals of level Shifted Phase Opposition Disposition PWM technique: There are 14 control signals obtained by multicarrier waveforms of level Shifted Phase Opposition Disposition PWM technique to get the 15 levels at the output.

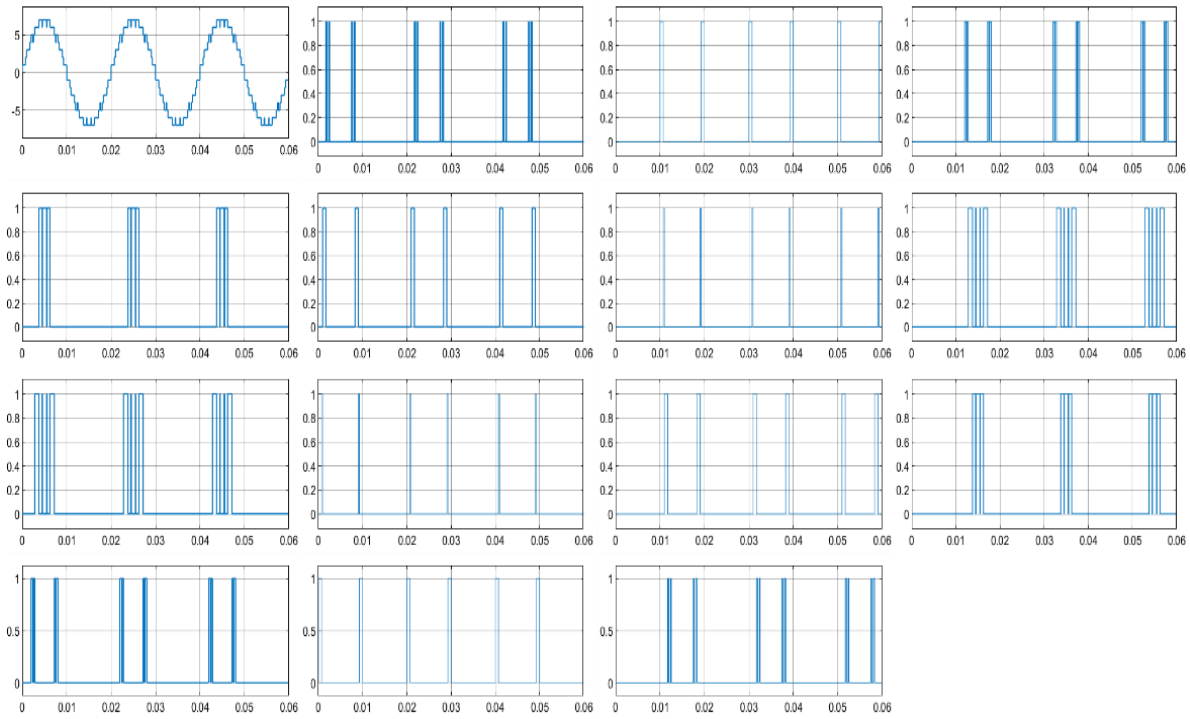

Fig. 6. Control Signals of POD MC PWM

III. RESULT AND DISCUSSIONS

The MATLAB software was used to develop the Cascaded H-bridge Sub-Multilevel Inverter based on three asymmetrical voltage sources. The diodes and asymmetrical voltage sources (12V, 24V, and 48V) have been used in the CHB Sub-MLI, 7 switches (IGBT) are used to get 15 levels output. Moreover, QS1, QS2 and QS3 followed by asymmetrical voltage 12V, 24V and 48V, respectively, used to contact the level generator. Polarity changer such as Q1, Q2, Q3 and Q4 used in the H-Bridge of MLI to get output, A logical circuit contains the OR Gate that feeds the signals to the MLI entrance to turn on the switches (IGBT). Two level-shifted multicarrier PWM techniques in the circuit have been implemented to get the desired voltage at the output that is 15 level output voltage. The THD is measured using the FFT tool of MATLAB software, as shown in Fig. 7 and Fig. 8.

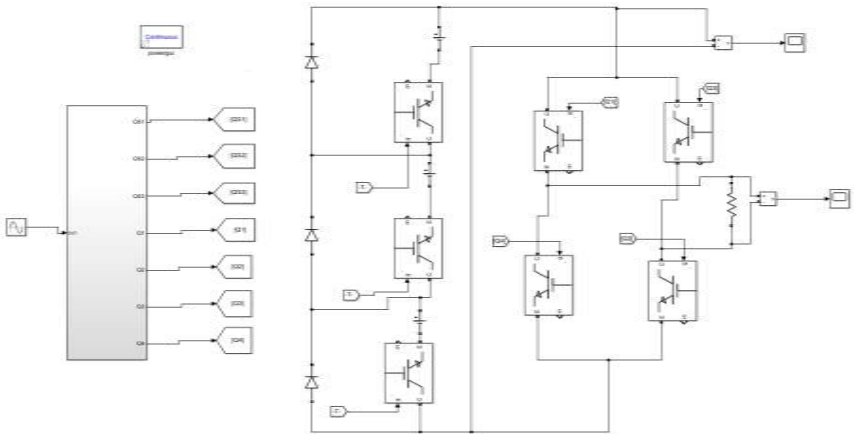

Fig. 7. A simulation model of CHB Sub-MLI

TABLE III
PARAMETERS USED IN MULTI-LEVEL INVERTER

Parameters	Specifications
Input Voltage	12, 24 & 48 V
Output Voltage Level	15 Level
Switch	IGBT
No: of Switches	7
Resistive Load	200 ohm

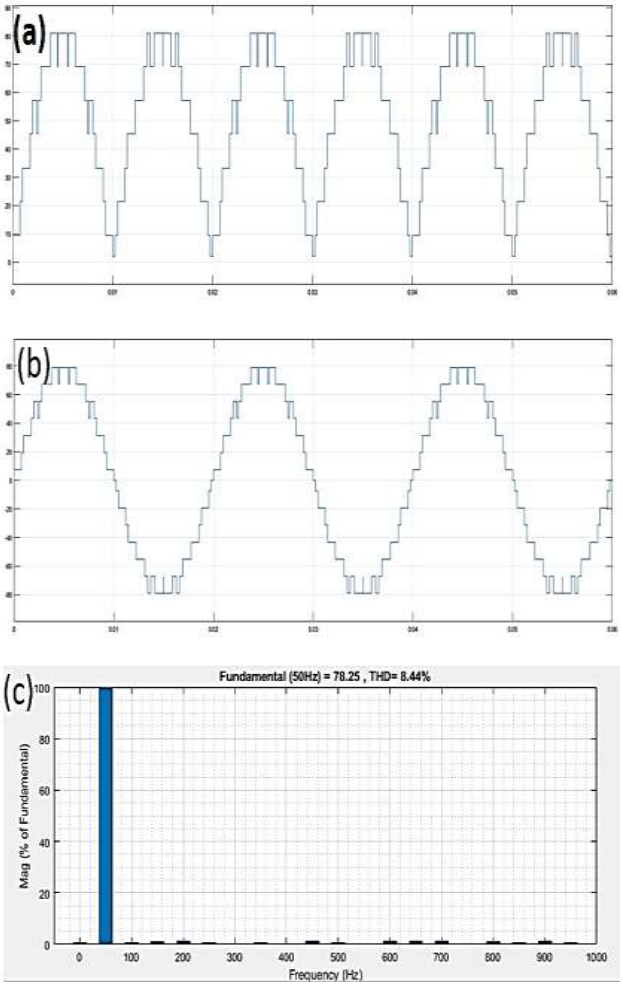

Fig. 8. (a) Level generator of CHB SUB-MLI (b) Output voltage waveform (c) THD of MLI on LS MCPWM

Fig. 8 part (a) shows the level generator of CHB Sub-MLI that is generated by switches QS1, QS2, and QS3 and it is connected with subcell of the voltage source, part(b) shows the Output Voltage waveform of 15 level output that is obtained by implementing the PD Multicarrier Pulse Width Modulation and the part (c) shows the THD = 8.44 that is got by the implementing the PD MCPWM.

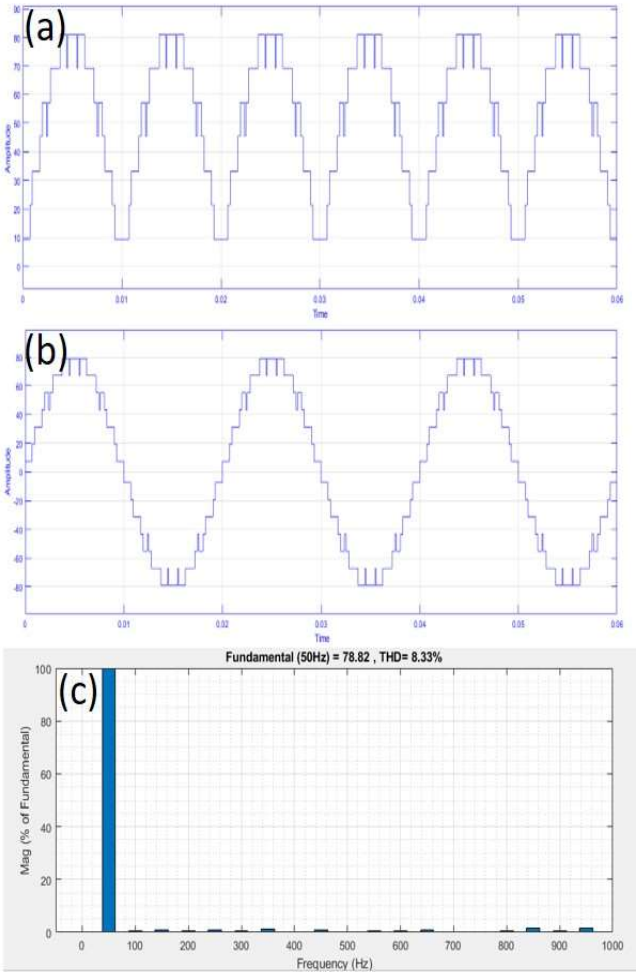

Fig. 9. (a) Level generator of CHB Sub-MLI (b) Output voltage waveform (c) THD of CHB Sub-MLI

Fig. 9 part (a) shows the level generator of CHB Sub-MLI that is generated by switches QS1, QS2 and QS3 are connected with subcell of the voltage source, part (b) shows the Output Voltage waveform of 15 level output that is obtained by implementing the PD Multicarrier Pulse Width Modulation and the part (c) shows the THD = 8.33 that is got by the implementing the POD MCPWM that are much smaller than the former.

IV. CONCLUSION

In this work, the simulation model of Cascaded H-Bridge Sub-Multilevel Inverter is successfully developed in MATLAB software. The Level-Shifted Phase Disposition and Level Shifted Phase Opposition Disposition Multicarrier PWM techniques are implemented with a Cascaded H-Bridge Sub-Multilevel Inverter. From the simulated results, it is concluded that Cascaded H-Bridge Sub-Multilevel Inverter with Level Shifted Phase Opposition Disposition Multicarrier PWM technique, has more accurate results as compared to LSPD technique.

Declaration of Competing Interest

The authors state that they have no known competing financial interests or personal relationships that may seem to have influenced the work described in this study.

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